U.S. Patent Application Serial No. 09/351,544

Declaration of Timothy K. Carns

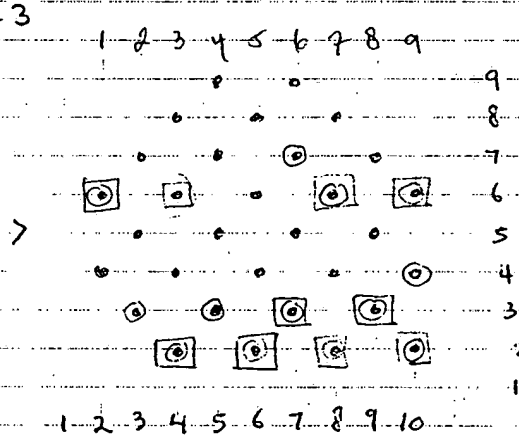
Document C

- Arrive work @ ~8:12am
- Read emails
- Start working on the PEVAL data / summary again for D1114.

Nplus
NPCONTY1 → Serpentine continuity

NP3RID1 = Vtfpnc

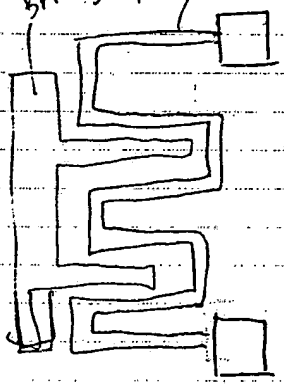
D1114-3



pt source drain

○ - wfr 3
□ - wfr 4

continuity test NPCONTY1 for n-channel devices

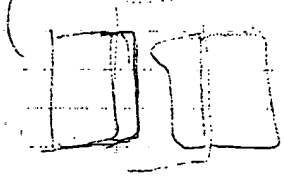


wfr 13 & 14

no implant
S-D spacing is low
Fox is thin

nwellrho

stripping back (top down) SEM cross-section



pt bridge continuity structure
Ask Scott

gate is shorted to S or D

broken wire is probably not a problem...
Look at PEVAL data more carefully.

9365 → 237235

~~K60~~ K16 lots of room than 402 (3×3)

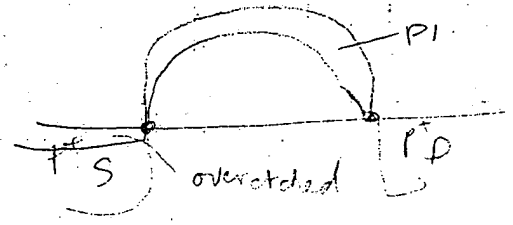
~~more~~ smaller due → more sensitive we have

'4.

Talk Scott – Layout structure, design violation

– BVDSFPP, LKGFPP look ok

– overetch P1 (L40)



if there is a layout problem, then we should see it more often

not a self-align gate, because it is a field device

p+ diffusion

diffusion to diffusion ~~short~~ is not violated

S D

$0.875 = \frac{3.5\ \mu m}{4}$ = min diff-diff space to get FOX in there

0.875 μm = minimum diff-diff space to get FOX between S & D

compensate (0.5→0.35 μm), no design violation

2.5, 0.8, 1

re

$V_D = 3.3\,V$, 3.5 V (max)

max potential of S–D

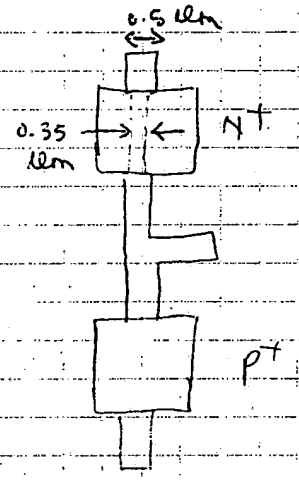
ii

CMOS CMOS
7223 = 7120

7235, well Vt implant is modified
well Punchthrough

$T_{gate\,ox}$ = 70 → 110 Å
Z37235

min poly line width ↑ from 0.35 → 0.5 μm



Z36223 & Z37223, the N+ device, the gate width is drawn 0.5 μm, but in the fab it is compensated to 0.35 μm.

The P+ device's gate width is NOT compensated.

In Z37235 device, Both N+ & P+'s gate width = 0.5 μm. They will not be compensated. What you see is what you get!

Field, V_D = 5V
NMOS, V_{DS} = 3.5V (max)

$\frac{3.5\ \mu m}{4} = 0.875$ — diff to

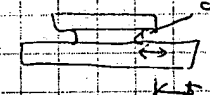
unless they are same pol & same mask

unrelated diffusion

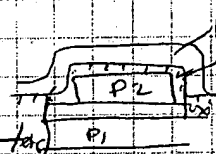
Capacitor Etched meeting 2pm : PI & UPD & M● groups
~~Meeting 2pm~~

Show D1261 has good capacitor but other problem arises, swing effect that PEARL had fixed, & now can not be fixed

Problem Avoidance
1. too many steps
2. redeveloping "
3. Don't recreate cap. leakage & ~~beff~~ yield sensitivity big sigma.
4. Do we want technician to distinct 737120 vs. 7223 flow

Solutions:
(1) Don't remove IPD (inter poly dielectric) at L39 "punch it" at L40, Lot 1168, 1549.
(2) Wet (50:1 BOE) IPO Removal at L39 has 50% overetch


3. Use 4528 dry removal w/ L39 in place w/or w/out resist in place
4. Flow layer 39 resist / Build more polymer / & 1 mask (no budget to buy) & we have etched tech to do this
5. ~~BARC~~ (needs a lot of development) ⇒ ∴ use it as back liner
6. If oxynitride (PECVD) then potentially = PEARL (1168 lot ~~1549~~) as the dielectric layer. Want to analyze 1168 lot before condering this option
7. ~~Return to the 6223 flow~~ (-)
(8) Seal edge w/ RTP or Dep/spacer etch
9. Use IPO as "ARC layer ~~(nitride/pearl/etc)~~
10. multilayer ARC (nitride/pearl/etc)



Leaving oxide under pearl is not going to work.
Swing effect >< big σ

Is it pearl between the poly plate or pearl

Questions: what are the experimental questions that needed answer

1. Leakage path due to oxide undercut, P2-pearl-P1 or P2-undercut-P1

2. quantify impact to BPSG CMP & contact etch.

3. what is σ difference for various conditions, vs. psc. IPD or NRC

4. Cost & complexibility (near & long term compatibility to E37223)

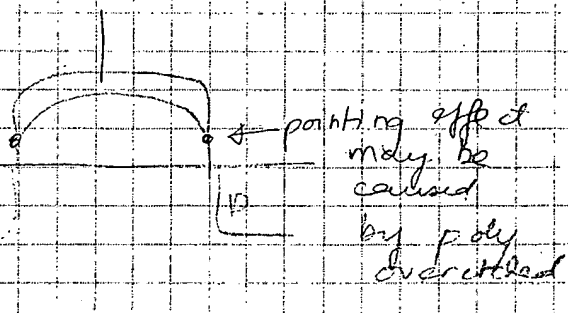
5. Are CMOS XTR's still happy

6. Meet all other measurables per psc (roll-off)

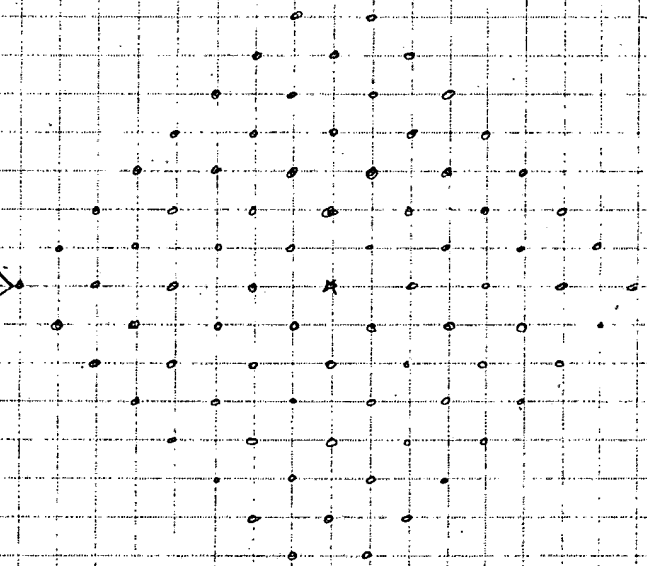
Factor	Action / Levels
* Pearl	Y N thickness
* IPO Removal (L39) from transistor	wet, dry, polymer, LE Mask, not doing anything
* Edge seal (method / thickness)	RTP, Spacer (deposition & spacer etch) 1000 vs 2250°A
* IPO Material	Thermal-, dep-oxide, dep-oxy, grow/dep ONO
* L40 Exposure	4 way / splits

Don't need waffles toward BPSG polishing

what have been done in D1168, D1261A & D1549 lots to narrow down these possibilities



poly overetched
→ cause Vtfppc to shift dramatically in D1114 (Summary report)

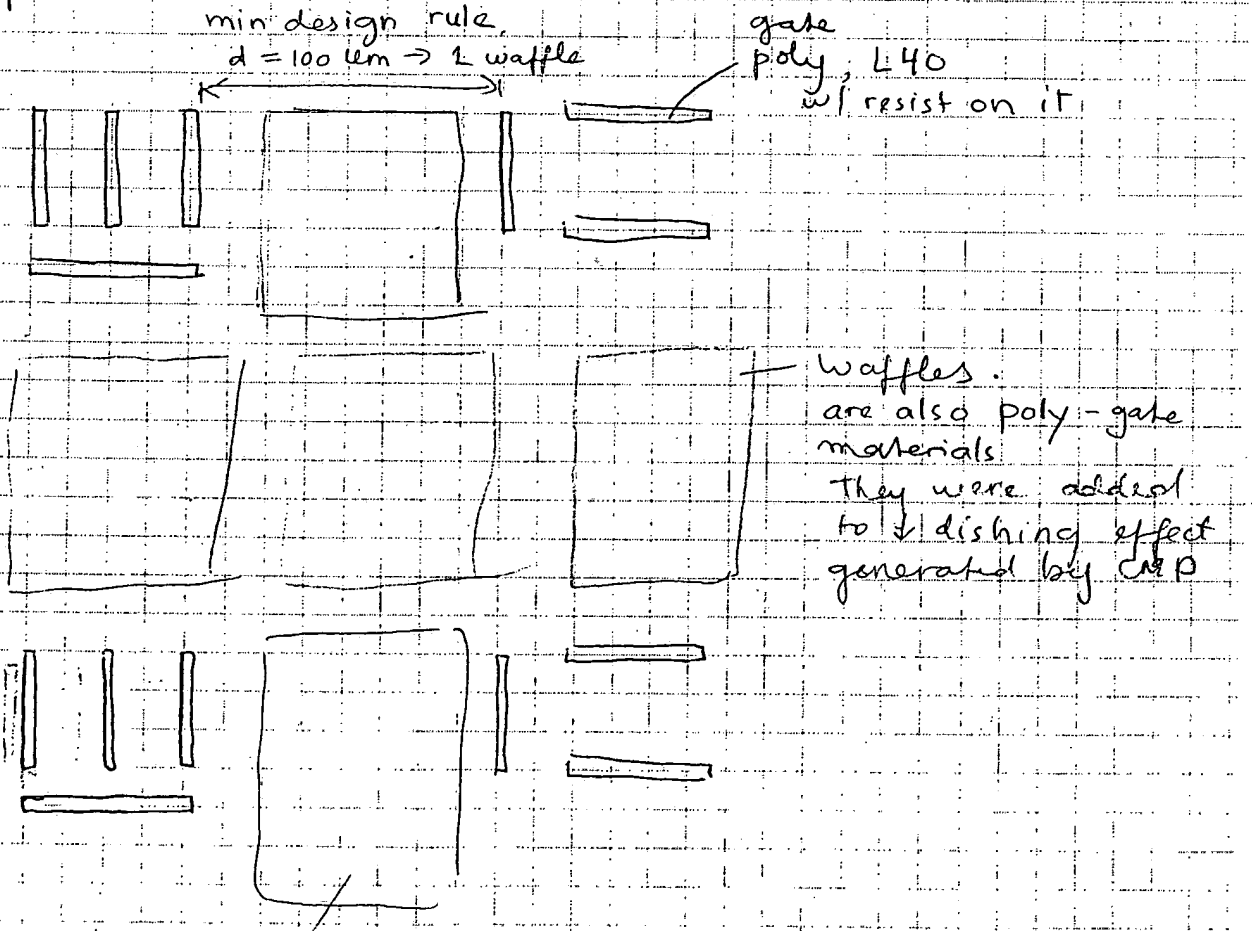


- Arrive work ~ 11:30 am
- Work on D1114 PEVA4 Summary report
- Got most of them done, except in Executive Summary & the poly-overetched stuff (w/ waffles) that may caused the field poly gate defects at/near the S/D ($I_g \gg I_d$)
- Left ~ 9:50 pm

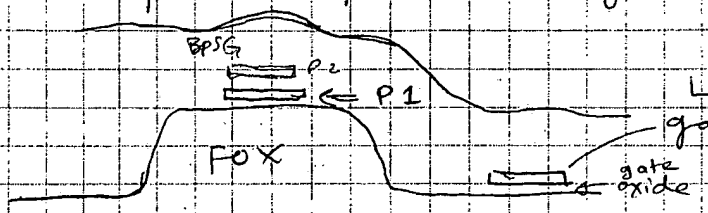
12/14/98, M

- Arrive work ~ 8:10 am
- Attend the 8:10 meeting → 8:35 am. J. Smythe mentioned that L-40 mask WITHOUT WAFFLES would be here today
- Call US West to pay bill $53.56 (not paid $ ~67 from budget call)
- Read emails → print out the email from John Smythe about the discussion on
- Work on D1114 PEVAL Summary report:
- Talk to Mike about overetch poly 1 (L-40) caused by putting waffles in the open / unused area to reduce the dishing from polishing (CMP)

In standard / normal Z-7o process, there is a lot of open area:

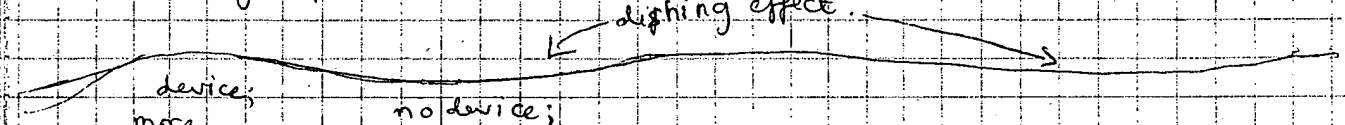


The previous picture is equivalent to:



As you can see that without waffles, a lot of poly mtl got removed @ L-40 etch. Typically 90% or more poly got removed.

Also without waffles, when polishing the wafer after BPSG 1 was deposited, the open / less dense area gets polished faster & deeper than the more dense area. This uneven polishing rate creates the so-called a dishing effect.



⇒ global dishing effect

This dishing effect can cause problem for leaving an unnecessary layer of mtl on a device, i.e., metal (W-plug) may not be removed completely, etc) ⇒ cause shorted device.

So, decision was made to add WAFFLES in the area where there is open area of 100 μm. Design role is to add a waffle where the gate poly are at least 100 μm apart (100 μm, 200 μm, 300 μm, etc.)

Waffles were added to reduce dishing effect.

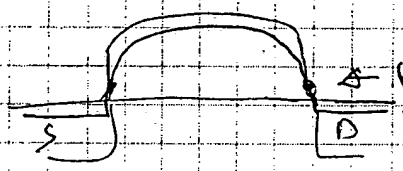
So now w/ waffles (= poly gate mtl), the total amount of poly gate removed at L-40 etch would be much less than there is no waffles.

With tremendously smaller amount of poly to be removed, there is so much reactive gas left in the chamber to continue etching the area not covered by resist ... ∴ Poly etched rate is much faster & thus deeper.
This faster etch rate, etch right through the gate oxide & attack the single crystal underneath it.
That's why we trench the substrate in lot D1114.

- The entire problem is caused by NOT adjusting the amount of reactive gases in the chamber w/ smallered amount of poly gate removal.

- Obviously, there is an etch rate difference for more vs. less dense area that can cause non-uniformity throughout a wafer. Typically, more dense area etched slower than a less dense area.

- Add the above discussion to D1114 lot report to support the large shift of VTFPPC that was thought to be caused by the field edge defect of poly gate & possibly caused by over etched poly gate to trenching the substrate.



high field trench into substrate caused by over-etch poly gate in D1114

- Got the report done ~12:30 pm, make copies & arrange the appendices. Go to lunch

- Gave the report to Mike ~1:30 pm. Ask Mike about the next priority. He told me to look at/think about what kind of split we can do (on top of D1261, D1168 & D1549) that can answer the problems/questions addressed on meeting.

- Ask Mike & Lee of the 1261, 1168 & 1549 split lists, go make copies

- Send a package out → go to shipping & handling.

- Around 2:15 pm, go to Bldg 1 to pick up the software for remote access from Armand Sermonia. He showed how to access my emails & MS's application a little bit. Make copies on the procedure to install the software.

- Back to Bldg 2, send out emails to Brett Lowe to see if he is going to SL. He is NOT.
Talk to Donna about the power off on 12/29/98 whether decision has been made as to let us take a vacation on that day or use as substitute. No decision is made yet.
Tim is in Israel the whole week.
So, I emailed Din informed him of the off day @ Zilog on 12/29
May need to arrange my traveling plans.

- Look at the split list of D1261, D1168 & D1549. Try to make some sense why certain splits were done.

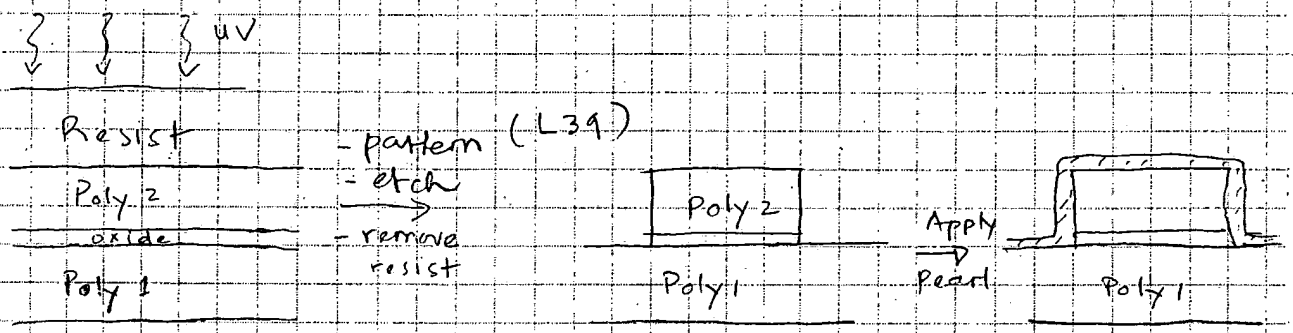
- This is my next project to see how we can answer the questions addressed on vetting) about the alternative cap-ox mtl, capacitor leakage & etc. In general, about finding a process that would be best for both transistor & capacitors.

- Wafers 13 & 14 from D1261A lot received thermal capacitor oxide twice, because the cap-ox strip step didn't remove all of the oxide (1 step runcard has wrong recipe name on it)

- Leave work ~7:05 pm!

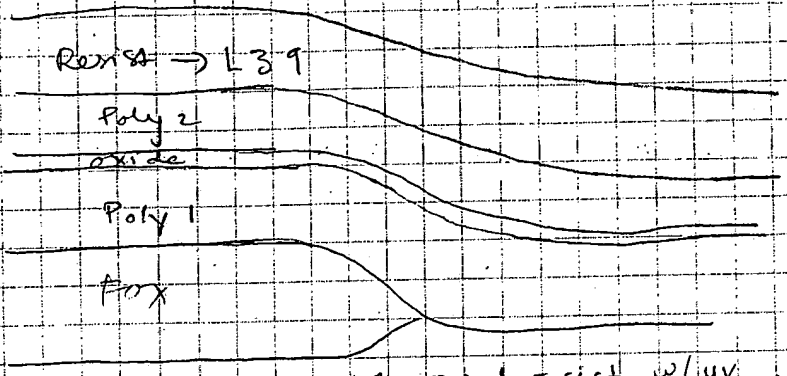
12/15/98, T

- Arrive work ~ 8:10 am.
- No mails
- Read Industry news distributed every Monday.
- Read the printout from John Smythe about the

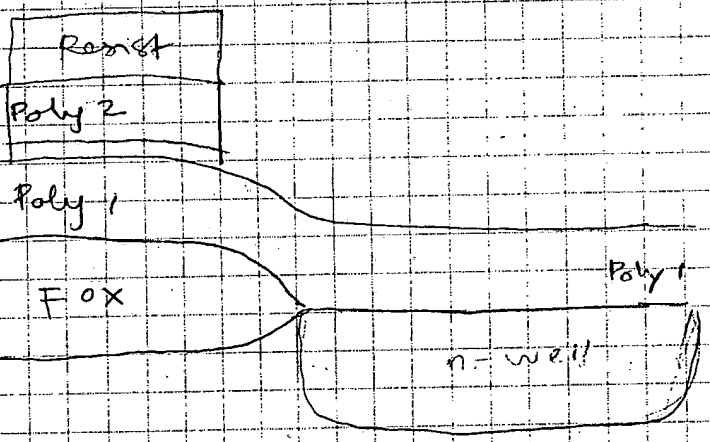


Pearl layer is directly on top of poly 1 ⇒ give good CD control of L40 exposure

D1114 (Initial L39 & L40 etch)

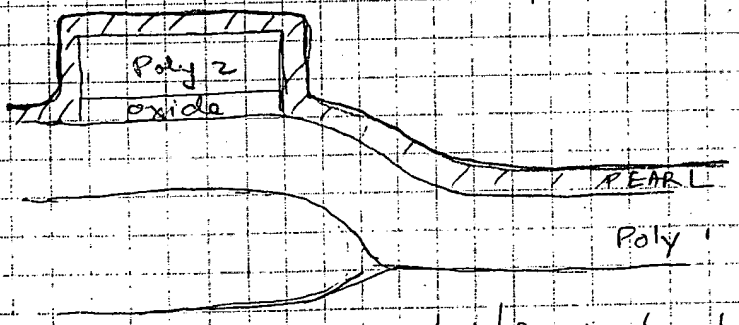


- exposed resist w/ uv
- pattern L39 (P2)
- etch P2 & IPO (inner poly oxide) removal using wet etch tech. The wet etch is used to remove oxide only.

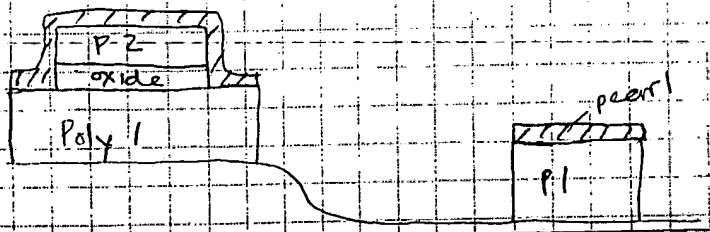


← VS. →

Remove Resist
↓
deposit ARC or pearl layer

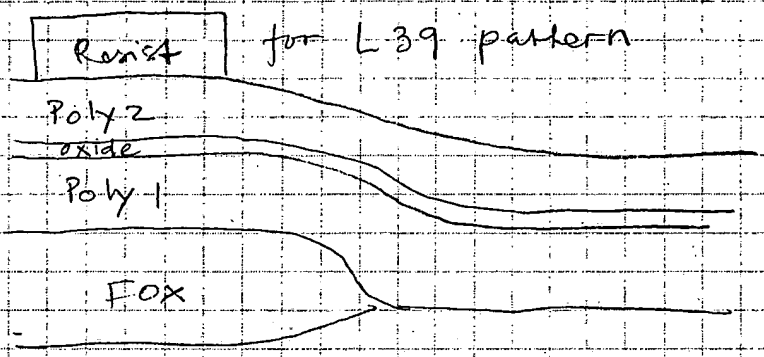


Apply Resist for L40 (P1) pattern



WITH PEARL directly on top of poly 1 → better/good control of CD @ L40 mask

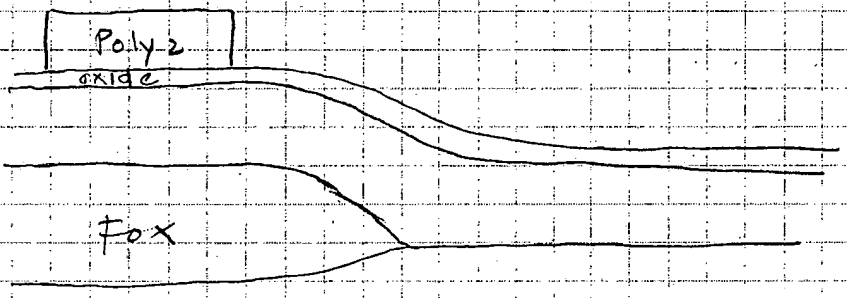
L39 & L40 etch proposed by John Horvarth



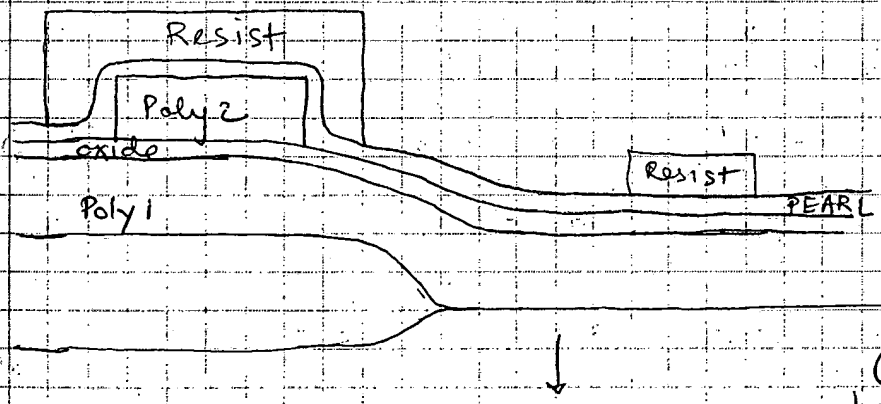
L39 → Poly 2

L40 → Poly 1

- Dry Etch Poly 2 ONLY
- Remove resist

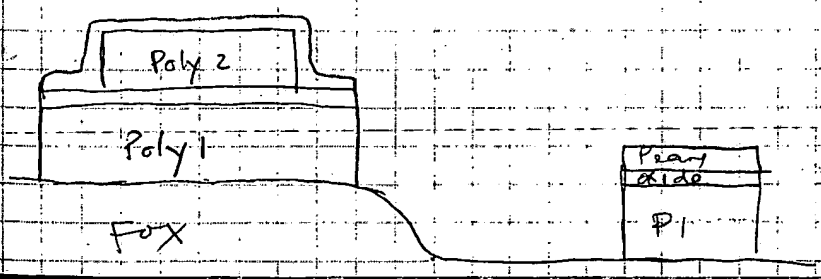


- Deposit PEARL
- Apply Resist to pattern Poly 1 (L40)



THEY CLAIMED that w/ PEARL ON TOP of OXIDE instead of poly 1 resulted in poor CD control @ L40

(As J. Smythe put it: Loss in swing suppression at L40 mask)



ARC = Anti Reflective Coating

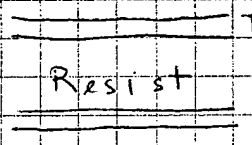
PEARL = Plasma Enhanced Anti Reflective Layer

Oxynitride, ONO

ARC = PEARL or pearl is part of ARC

ARC can be * organic (contains Carbon) (can be removed)
* inorganic (TiN; oxynitride or nitride) (can not be removed)

BARC = Bottom ARC
TARC = Top ARC



ARC is a generic term
PEARL is the trade-mark name of Novellus film
PEARL is used to improved line-width of photomasks (better control of line-width)

PEARL is Si-rich w/ some oxygen & Nitrogen.

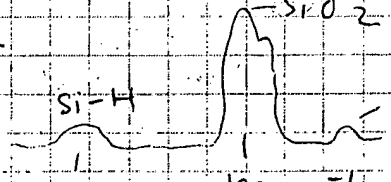
PEARL ⇒ SiO_xN_y (Si-rich), $SiO_{1.99}N_{1\to 1\frac{1}{2}}$

I've talked to Jim Shen, Brett Lowe & John Smythe; no one can tell me what the pearl composition is.

Typically (@ Zilog), PEARL is deposited using a PECVD. Although thermally grown PEARL is also possible using LPCVD (Low pressure chemical vapor deposition) tube at ~650-700°C?

Pearl has refractive index: $n = 2.4$ & $k = 0.5$ ⇒ ∴ Both n & k are important

FTIR



Si-H is observed when there are dangling bonds

$n = 2.3$ (@ $\lambda = 633$ nm, expose @ 365 nm). This is the only λ that they can measured n

$n = 2.3$ (@ 633 nm) ??
$n = 2.53$ (@ 365 nm)

n will tell you how fast the light passes thru a medium

k is absorbance / loss

$n \pm ik$

Pearl is typically deposited @ 13.6 MHz (high frequency). The Novellus system can only operate at this frequency.

Oxynitride is deposited using the same chamber as PEARL ⇒ PECVD. But the gas ratio of SiH_4, N_2O & NH_3 are different. (using both high (13.6MHz) & low (400-410kHz) freq)

Oxynitride is NOT rich in Si, it is a natural IPD (inter Poly Dielectric). From the name, oxynitride, I wonder if it rich in oxygen & nitrogen?

It contains SiO_xN_y, it is a one layer of SiO_xN_y

$n = 1.75$ & $k \approx 0$

Oxynitride can also be thermally grown using LPCVD tube at ~ 650 - 700°C

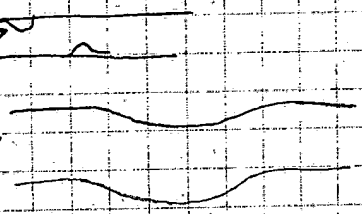
ONO = Oxide, Nitride, Oxide ⇒ 3 layers of film
SiO_2, Si_3N_4, SiO_2

Si_3N_4
Oxide

Oxide (much thinner because oxidation rate of Si from Si_3N_4 is much harder)

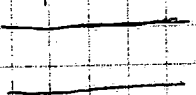
Without Pearl, when a material is going thru a photolithography step, we see:

- reflective notching
- thin film interference



In general w/o pearl ⇒ non-uniform layer after exposed

WITH Pearl, the above optical problems were reduced ⇒ more thickness uniformity

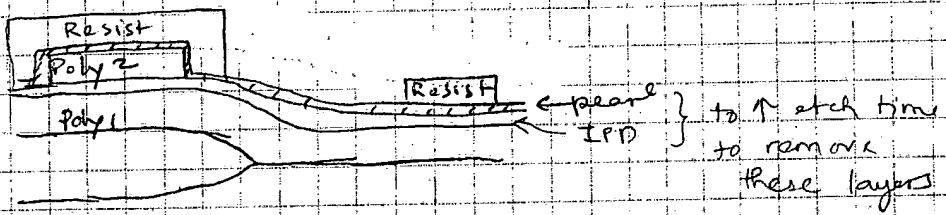


- Ask Mike about the notes - several words/terminology

IPM = Identical Process Module
SPM = Similar " "

Loss in swing suppression @ L40 mask ⇒ poor CD controlled

↑ Length of punch-through step in L40 ~~at~~ account for PEARL + IPD
= ↑ the etch time



Mike also mention, typically it takes a lot of justification to add an extra masking. Yet in the "comparison of Approaches by Step" (note from Smythe) indicating that there is a new mask level for the under-exposed L39. About 4-weeks ago when the new mask was proposed, most people against it & prefer the J. Horvath etch proposal; yet it looks like now Tim & John S. do not want to use Horvath etch tech, but want to do s.t. else.

- Leave ~ 6:20 pm

⇒ The transistor & capacitor from D1261 lot look great. D1261 used J. Horvath etch proposal to etch L39 & L40.

12/16/98, Th

Arrive work around 8:12 am
Read & response emails
- I'm going to start doing the split list based on the discussion or meeting we have

The last couple days I have been looking over the split list done on D1168, D1549 & D1261A to see what we are trying to accomplish by doing that splits, hopefully to not redo it again.

Split list of D1261A for 87L02 Capacitor Oxide Etch:

Wfr #	Cap. Oxide	Cap. Ox Etch	L40 - Expo Split	L40 Etch	Hook
11	Thermal	BOE	Yes	D1114	D1114 wf 2
12	"	BOE	yes	GOLD	
13	"	Horvarth	"	Z7223L40	
14	"	"	"	Z7223L40	
15	"	"	"	Z7223L40	
16	Novellus	130E	"	D1114	D1114 wf. 4
17	Novellus	BOE	"	GOLD	
18	"	Horvarth	"	Z7223L40	
19	"	"	"	"	
20	"	"	"	"	

Wafers 14 & 15 received thermal oxide twice because the one step runcard had the wrong recipe to remove the capping oxide (⇒ not all oxide of removed)

D1261A didn't receive L40 DICD splits on a wafer. However, the PEVAL data show that we have data down to roll-off region. According to Mike, it is the different etching at L40 causes different L-eff. (Maybe not enough polymer to protect the nearby surrounding.)

* Split list of D1549 capacitor oxide Etch:

wfr	Cap. Oxide	Cap Ox. Etch	L40 DICD split	L40 Etch	L50 Etch	Hook
1, 11	Thermal	BOE	Yes	D1114	D1114	D1114 wf 2
2, 11	—u—	BOE	Yes	GOLD	D1114	
3, 13	—u—	Horvarth	Yes	Z7223L40	Horvarth	
4, 14, 21	—u—	—u—	No	Z7223L40	—u—	
5, 15, 22	—u—	—u—	No	Z7223L40	—u—	
6, 16	Novellus	BOE	Yes	D1114	D1114	D1114 wf 4
7, 17	—u—	BOE	Yes	GOLD	D1114	
8, 18	—u—	Horvarth	Yes	Z7223L40	Horvarth	
9, 19, 23	—u—	—u—	No	—u—	—u—	
10, 20, 24, 25	—u—	—u—	No	—u—	—u—	

The split lists of D1261A & D1549 are very similar, except the additional split on L50 etch for D1549.

From these 2 lots, if everything runs as it should be, we should be able to distint the following:

* thermal vs. Novellus
* Buffer Oxide Etch (BOE) vs. Horvarth Capacitor Ox. Etch (wet etch for IPO removal at L39) at L39
* L40 DICD splits on a wafer will determine roll-off
* L40 etch (D1114, GOLD & Z7223L40) may still need to be optimized as they seem to shift the most of Left outside the spec window = 0.33 ± 0.05 um
* The L50 Etch (D1114 & Horvarth) in lot D1549 may also need optimization (no PEVAL data yet at this point). But L50 etch splits were added in D1549 to take into account longer / higher rate etching for having Pearl & IPO on poly 1.

16

Split List for D1168 is too much work to list. So, see the original split is. Except wfrs 8 & 16, the rest of wafers receive no IPO removal at L39 (Horvarth etch).
Again, if everything is going ideally, then we should be able to differentiate the following:

- Thermal vs. Novellus ONO Bottom Oxide (320°A)

  Thermal vs. Novellus hook back to D1114 (wfr. 8 & 16)

- Using oxynitride as IPD vs. ONO & Oxide

- For Novellus Bottom Oxide: (a) WITH TOP ONO oxide vs. WITHOUT TOP ONO oxide

  wfrs-received top ONO oxide (thermally grown): (b) time & temp (850 & 970C)
  (10 min vs. 176 min)

- For Thermal Bottom ONO oxide:

  (a) With Top ONO oxide vs. NO top ONO oxide

  (b) Wfrs that received thermally grown TOP ONO oxide:
  time (10 min vs. 176 min) = 5224 process @ 970C
  temperature (850 & 970 C).

- For Oxynitride IPD (all have 530°A thick):

  (a) WithOUT vs. WITH TOP ONO OXIDE. The wafers that received top ONO thermal oxide @ 850C for 10 mins will be tested because of this extra thermal cycle.

  (b) Annealing after oxynitride deposition (wfrs 17-25) & thermal top ONO oxide (wfrs 19, 21 & 23); distinct different annealing condition:

  40% N_2O TVF01 (tube) @ 850C - 10 min vs. N_2O RTP @ 1050C for 40 min. vs. 100% NH_3 @ 850C for 10 min

- L40 DICD split → roll-off analysis.

* Generate the split list
Divide the split list from J. Smythe into 5 splits

Comparison of Approaches by Step

Approach Number											
IPD Material	Ox	Ox	Ox	Ox	Ox	Ox	Ox	Ox	OxNit	ONO	ONO
Poly 2 Dep	X	X	X	X	X	X	X	X	X	X	X
Poly 2 Imp	X	X	X	X	X	X	X	X	X	X	X
Poly 2 Anneal	X	X	X	X	X	X	X	X	X	X	X
Deglaze	X	X	X	X	X	X	X	X	X	X	X
L39 Mask	X	X	X	X	X	X	X	X	X	X	X
L39 Poly Etch	X	X	X	X	X	PMR	PMR	X	X	X	X
L39 IPD Removal	B/D	B/D	B/D			B/D	B/D			DO	
L39 Resist Strip	X	X	X	X	X	X	X	X	X	X	X
New Mask				UE	UE						
IPD Removal				B/D	B/D						
Resist Removal				X	X						
Spacer Oxide		RTP	DEP	RTP	DEP	RTP	DEP				
Spacer Etch			X		X		X				
PEARL Dep	X	X	X	X	X	X	X	X	Y/N	Y/N	X
L40 Mask	X	X	X	X	X	X	X	X	X	X	X
L40 Etch	X	X	X	X	X	X	X	PTD	PTD	X	PTD
		#1		#2		#3		#4		#5	

B=BOE, D=DRY, UE=UnderExposed L39 mask; PMR=L39 etch with added OE polymer;
PTD=L40 etch with punch through increased for IPD+PEARL; Y/N=WITH/WITHOUT;
DO=Dry ONO etch

Combine Splits 1 & 3 ; split 2 & 4 ; split 5.

If we actually going to do all of these three splits, need to know the following:

Split 1 & 3 :

SDE: Statistically Design Experiment for L39/L40 on 87L02 } this is actually what my project is called → to do the split list stuff.

- Go over the split list w/ M. Westphal. There are a few suggested changes: Horvath → actually L39 resist strip only
  Add the hook wafers #
  ~ 5pm → 5:30 pm

- Send out those split list (capox_split1&3, capox_split2&4, & capox_split5) to Mike, John & Tim. This is what I say in the email:

  Attached are the proposed splits for L39, IPO, L40 RT on 87L02 based on the table below (J. Smythe). I group the table into 5 major splits. Split 1 = the 1st 3 columns (reading from left to right), split 2 = col 4 & 5, split 3 = col 6 & 7, split 4 = 8 & 9, & split 5 = col. 10 & 11. It looks like 3 lots will be sufficient to do all splits.

  Feel free to make comments & suggestions on the proposed splits & let me know of any changes you would like to see. Thank you.

  This email was sent out around 6:38 pm.

- Leave work around 6:45 pm.
- Go to Albertson's directly to buy some ribbon or bows & cards, but couldn't find a good deal. So I went home to have my dinner & then went out again to Paul's grocery store to buy those items

- Making cooky dough from ~ 9pm → 12pm.

12/17/98, TH

- Arrive work at 9am. Pretty tired so I woke up late from making cookies dough last night
- Let Donna Lowe knows (~8:20 am) that I'm going to be late.
- Talk to Mike about what I should do next. Nothing much.
  - He told me to go ahead send out a meeting notice to every-one to discuss the split list for 87L02.
    - → so I did
- I tried to log in to WHITE to learn how to create a new STR. I was not successful.
- Might want to ask Scott about the status of TDC for me to analyze (do manual measurement) on the new SLM of 87L02 (Z37223).

  Last several SLM meetings were focussed on new SLM that can be used for double (Z27223) & triple (Z37235) layer metals.

- Send out Christmas card for Tim, John & Pete.
- Will bring cookies to Donna, David, Lee, Mike, Thomas, Scott, Arnin, Shawn, Bee, Deb Acuck, Jean & Margurit, Min, Jim & ~~Kuo-Lin~~ tomorrow
- According to Mike that we are still waiting for D1168 & D1316 PEVAL data. So there is not much to do.

- The meeting notice was sent out to: John Esposito, John Horvath, John Gold, Britt Lowe, Mike Westphal, Steve Buffat, Jon Daley, Lee Debruler, Thomas Chung, Bee Kickel, John Smythe, Tim Lams, Min Huang & Alan Vonkrosigk.

  The meeting will be tomorrow at 10 am in Blue Room.

- Think about why certain splits were proposed, how the previous splits (D1261, D1168 & D1549) can answer some of the questions (so no redundant will be done hopefully), how the current splits can answer those questions as well.

- see a doctor from 1:30 → 3pm. Have to argue w/ them that I have an insurance, even-though I don't have the card yet. Dr. Asadorian wants me to set up an appointment w/a physical therapy. I called the physical therapy office, have an apt at next Tuesday at 8:15am at the MOST therapy center nearby Mercy Hospital

- Rest of afternoon, play w/ generating a new STR. Called up Wendy on how to log in. Got most of help from Mike while Thomas watched us.

- Asked Mike what I should do for the meeting tomorrow

- ~~A~~wait

12/18/98, F

- Arrive work ~8:05am
- Distribute christmas goodies till around 8:25 am
- Back on looking at the proposed split lists & thinking how to present them at 10 am meeting.

- Mike came talk to me and tell me to spare the details (i.t.o. thinking the split lists).

- Shawn came talk to me about the topic: why when we already knew that wet etch causing bin undercut of oxide below P2. I don't know how he knew. My guess is Mike might have told him this issue & told him to come talk to me so I get some-kind of practice before the presentation.

- Meeting at 10 am to review the split list. Jon Daley, Bee Kidd, John Esposito, John Gould, Brett Lowe, Jim Shaw, Min Huang, Lee Bebtiller & Mike Westphal attended the meeting.

John Smythe didn't attend even though he accepted the meeting invitation. I went to look after everybody in Blue room waiting for him. He was not at his office, so I asked operator to page him. Later Donna came told us that he is bldg #1 w/ Pete Nanos to meet w/ Mike Bradshaw. They were there from ~9:45am → ~1:15pm.

The meeting didn't go well. I couldn't bring everybody's discussion together. John Esposito went to bring a marker for me, so I could mark what we don't want to do. I felt pretty stupid because I could NOT bring everybody together. Brett was the main speaker. Probably, he did it on purpose because I might have upset him when I asked him question about PEARL vs ARC vs oxynitride on Tuesday (12/15/98) (n & k @ particular λ = 633 ? 325nm)

Mike also presented D1261 box plots (BVDSS, Leakage) that D1261 has much higher BD & low/unmeasurable leakage @ ?5 V because this lot received L-39 resist removed only, oxide & L40/poly were removed by dry etched. Based on this data, Esposito & the rest of people said that all we need is a much simpler split from the one presented by Smythe. It came down to split on RTP vs. Deposited oxide for BOE oxide RTP oxide for BOE & Dry Etch.

Went to lunch @ Hong Kong

I started working on split list proposed from the morning id dvt meeting

At ~ 3 pm received priority lists from Mike & Thomas & learned that my 1st priority to do Roll-off @ L10 for D1315

- D1315 downloaded from hp → RS1

Learned from Mike to combine all data into 1 giant table.
add rows to newtablename from filename_of the data
Combined all data into D1315 tablename.
Noticed that wafer 14 has 2
wafer 14 has a lot of bad site : Leffnc (col 22) = -2×10^{33}
Delta L1 (col 23) = ——

(one or two bad sites) Leffpc (col. 48) = -2×10^{33}

Looked Leff data, there is not much variation from 1 wfr to another. So, I didn't know what I should look at the roll-off parameters (BVDSS, Leakage, etc) against
And Everybody already gone & give up for today

- Left ~ 6:40 pm

12/24/98, M

- Arrive work ~ 8:10 am
- Attend 8:10 meeting → 1st priority is to do D1315 L10 roll-off report
- At 8:24 am read emails
- Talked to Mike about what I am suppose to do at the L-10 roll-off. what parameters) to look against

* For L-10 roll-off, the parameters to look at are the same as typical (L40-CD splits) roll-off but against NP_W (= N+ width).

Typical L-40 CD → Roll-off will be looked at against Leff @ L-40

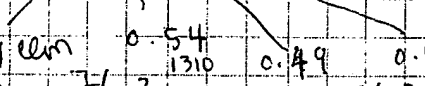
→ Assume PP_W (= P+ width) is controlled by the same level as NP_W.

* Wafers 1-10 received Z37120 process (no capacitors)

wafers 11-25 —— Z37223 process. The difference between Z37223 Vs. Z37120 is the capacitor oxide & poly 2 on Z37223.

* wfrs: 11-15 , 16 → 20 , 21 → 25
L10: A B C

L40 CD: 4 splits , 4 splits , 4 splits
split



0.59 um 0.54 1310 0.49 0.44 um
Exp = 1240 /m² 1420 /m² Exp = 1560 /m²

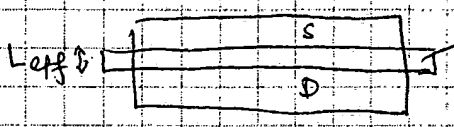
Want to look at wfr 11-15 1st to look at L40 CD split
16-20 2nd to
21-25 3rd to

For each L40 CD = f (L10 splits)

24

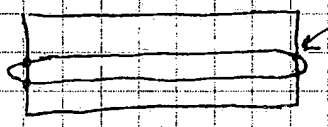
* The reason we are increasing L-IO width is because it is thought that the rounding around the edge of the gate causing a poor roll-off performance.

Ideally, we want to have a perfectly uniform & sharp edge of gate.



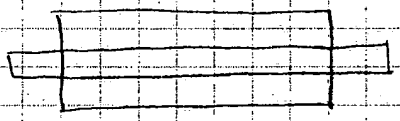
No change in Leff throughout

Ideal case



smaller Leff at the edge may cause for a poorer roll-off performance

Real World Case



Pearl layer should take care of the rounding edge effect.

Typically n-channel poly gate width is compensated from 0.5 μm → 0.35 μm

p-channel poly gate width is NOT compensated

std1315.hp = wafer 1

std1315_a.hp = wafer 2

std1315_b.hp = " 3

_c.hp = " 4

_d.hp = " 5 → 6

_e.hp = " 7

_f.hp = " 8

_g.hp = " 9

_h.hp = " ~~10~~ 12

_i.hp = " ~~12~~ 13

retest _j.hp = " ~~13~~

some parameter shift

_k.hp = " ~~14~~ 15

_l.hp = " 17

_m.hp = " 18

_n.hp = " 19 → 20

_o.hp = " 22 → 23

_p.hp = " 24 → 25

std1315_q.hp = " ~~15~~ 14 (use this file)

Wfr 11 was pulled after P1 - deposition for AFM

Wfr 16 was pulled out for AFM analysis (after P1 anneal)

" 21 " " " after Capox Deposition for AFM

Wafer 15's data got shifted by 1 col, approximately col 5 → 8. Later Lee fixed that, so I don't need to shift it or guess which col is for which.

col 3 = VTLEXN_1

col 29 = VTLEXP_1

~~d1315.hp~~ = wafer # 15

PEVAL wfr 10 → 12

PEVAL retest 12 & 13 are the same = 13

make boxplot junk from col ? to col ?

10 → 12

12 → 13

W/o OPC → lower Left

- don't want to use 13 because it is a retest.

d/s col 81 to 85 ? = where col 13

col 11 = VTLENC ✓
12 = GMN_2
13 = GAMMA2
14 = VTON 2
15 = VTSEXN_2
16 = IOFFN2
17 = SN_2 ✓
18 = IDSANC
19 = BVDSNC ✓
20 = IBSN_2A
21 = DIBLN
22 = LeffNC
23 = Delta_L1

97 = MP_W
99 = PP_W

1 = wafer

col 36 = VTSEPC
37 = GMP_2
38 = GAMMAP2
39 = VTOP 2
40 = VTSEXP_2
41 = IOFFP2
42 = SP_2
43 = IDSAPC
44 = BVDSPC
45 = DELTA_W2
46 = IBSP_2A
47 = DIBLP
48 = LEFFPC
49 = Delta_L2

SN_2 vs. LeffNC VTSENC (μm)
BVDSNC vs. LeffNC VTLEXN_1 (V)
IOFFNC vs LeffNC
BVDSNC vs IDSANC
VTLENC vs LeffNC

IOFFN2 has a lot of huge # ~~1e⁻⁷~~ → 1e⁻¹¹ data that I got rid off. ⇒ on wafer #14

SN_2 & SP_2 also got rid off data pts = 1.7e³³

SN_2 most bad sites occured for wafer 14
There is one (-) # (~-427) occured for wafer 15 (SN_2)

DIBLN has a lot of -4e³⁰ pts for wafer 14

IDSAPC remove ~~0~~ e⁻¹⁰ data pts

IOFFP2 remove -e⁺⁷ → -e⁺¹⁰

Through out the day, generating plots from these table:

D1315A (wfr 12-15) L10 DICD = 0.8 μm, Exp = 1600 J/m²

D1315B (wfr 17-20) L10DICD = 0.9 μm, Exp = 1450 J/m²

D1315C (wfr 22-25) L10 DICD = 1.0 μm, Exp = 1200 J/m²

12/22, Tuesday

- Went to see a physical therapist from 8:15 → 9:30am
- Arrived work work ~ 9:35 → 9:40am.
  Went directly to the PI-group meeting at 9:30am until 11 am

From the meeting, I learned these are my priorities:

* D1315 L10 / Pearl Splits, Lot Report L10 roll-off sensitivity is my 1st priority.

  Want to resolve ΔW effective issue. Want to ~~go~~ get this issue out of the way.

* D1815 Lot Analysis Well Anneal is my 2nd priority.
* I-V-T on SLM07/09/55 (D1114) may be my 3rd priority. This is a clean up issue.

Global priority:

1. Lot 1549 → will tell us the unit process of L-40 etch.
2. D1315 (SV)
3. STR: 7223 IPO Removal STR L39/L40

Tim wanted to go over the split list for L39/L40 STR at 3:30pm.

The plots generated are

Boxplots V_{tlexn_1} (V) vs. wafer #
" V_{tlexp_1} (V) vs. wafer #

VTSEXN_2	vs.	Leffnc	(sort = wafer #
BVDSNC	vs.	Leffnc	(" = "
BVDSNC	vs.	IDSANC	(" = "
IOFFN2	vs.	Leffnc	(" = "
SN_2	vs.	Leffnc	(" = "
VTLENC	vs.	Leffnc	(" = ")

VTSEXP_2	vs	Leffpc	(sort # wafer #
BVDSPC	vs	Leffpc	(" "
BVDSPC	vs.	IDSAPC	(" ")
IOFFP2	vs.	Leffpc	(" "
SP_2	vs.	Leffpc	(" "
VTLEPC	vs.	"	(" ")

For each group of L-10 CD, each wafer received L40 DICD. ⇒ L10-CD = f(L40-CD)

- Leave ~ 7:10 pm

- Showed Mike those RS1 plots that I generated yesterday.

The interesting part is that the roll-off (L-40 CD) only occurs for a particular wafer, even-though all wfrs (15 → 25) received L-40 DICD by row.

- L40 DICD by row :

	Leff Targets
0.472	0.38 (1)
0.425	0.33 (2)
0.377	0.28 (3)
0.32	0.24 (4)

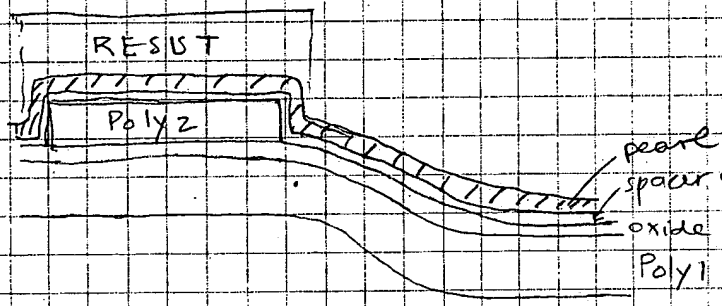
- Generate a Table D1315_L10 to see which set of data for each wafer that received the same L40 DICD split.

Wafer #	split	Leffnc	Leffpc
12	(1)	row 2, 8, 10, 16, 18, 20, 26	
	2	row 4, 6, 12, 14, 21, 23, 29	
	3	row 1, 3, 9, 11, 17, 19,	
	4	row 5, 7, 13, 15, 22, 24, 28	
		row (Leffnc)	
13	1		
	2		
	3		
	4		

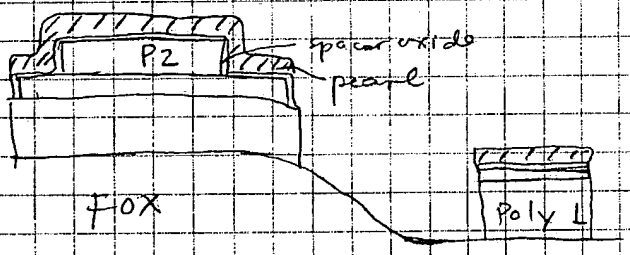
12/23/98, Wed.

- Arrive work ~ 8:15am
- Find a X'mas gift on my chair. It was from David Lee.
- Will work on the split list that Tim & I & Mike discussed about yesterday.

Wafers 1 & 2 do not receive spacer oxide step



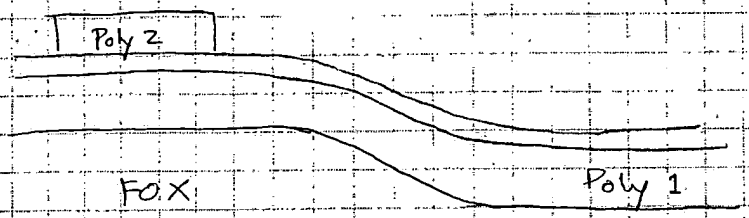
↓ Horvath
Etch @ L40
→ Remove resist



= D1261

PEARL IS NOT TOUCHING BOTH Poly 2 & Poly 1

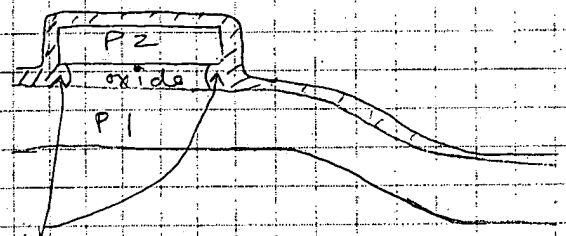
After L39 mask & poly etch



↓ BOE (wet etch oxide)

* Spacer oxide (RTP or Dep.)
* Etch the top layer of oxide
* Pearl Deposition

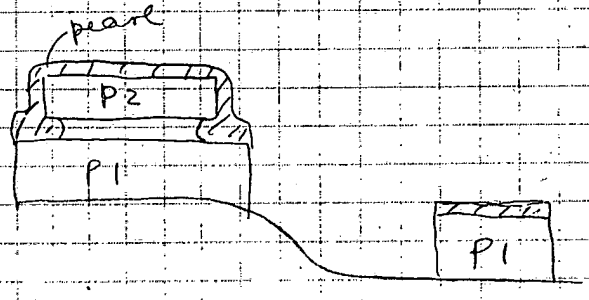
Pearl Dep

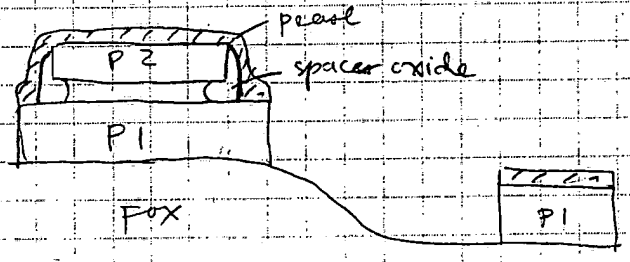


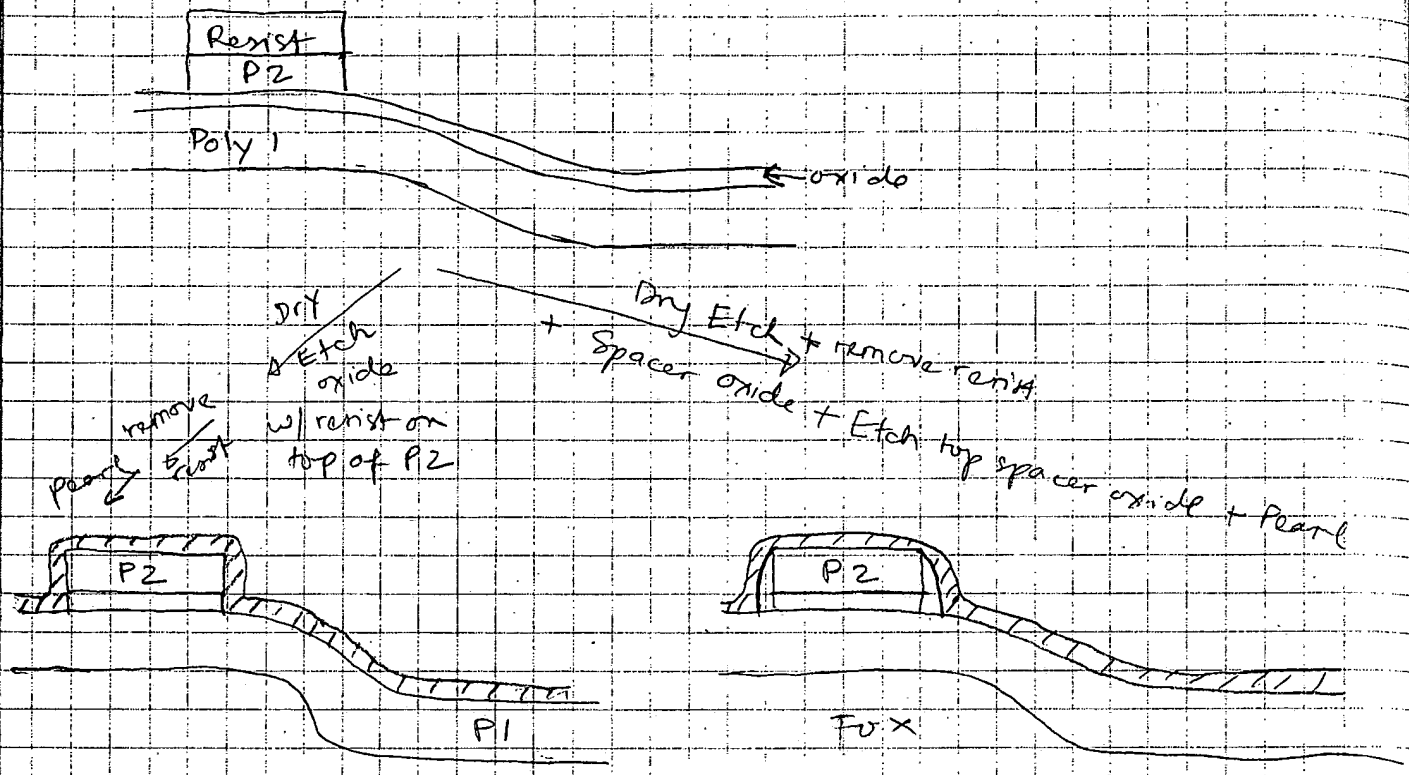
This void could be filled by L39 resist &/or pearl

= wafer 7 (= D1114, wfr 2 = thermal
wfr 4 = Novellus)

↓ L40 mask & etch would be 1R2 same as D1114 (pearl + P1 only)







pearl on both P1 & P2 ⇒ may be leakage path.
If this is the case then having spacer ox is not going to solve the leakage path

dry etch, RTP, 1000 A, 2250 A oxide ⇒ 4 possibility of spacer & etch.

12/30/98

* Went to see a doctor from 8am - 8:45am

* Arrived work around 9am

-

* Meeting @ 9:15 w/ Tim, Thomas, Mike, David & Sanjauti
  - Wafer 15, 20, 25 didn't have leakage capacitor problems from D1315 lot. => have BOE oxide

  Pearl contacts both poly 1 & 2 => leakage path

* Next year project, current schedule to meet the deadline
  Hit a technology at a time (7223, 7235) & see what need to be done (at least limited release)
  production > LPR

  Z37223
  L.P.R = 01-11-99
  contingent: ① one lot through
  500x temperature cycle, needs:
  - wafers
  - test program
  - final test
  - burn-in board
  - STWR

  } D1550 will force these items to get done. into qual.

Rubin, Zippi names were mentioned.
We can use D1549 as Quality item as well as a back-up wafers

D1550 = call it "Qual 1"
D1549 = Qual 2

② Need D1549, data D1315 (capacitor), D1168 SGIR's STR
Esposito didn't have objection for limited release based on several wafers' results

Take capacitor from D1549 & D1315 (wafers that don't have undercut w/ pearl) & also transistor (L40 splits — Leff) data as well
But, mostly focus on capacitors

Need lot repeat on D1549 & D1315.

③ D1168 is not on a critical path for limited release based on D1549 & D1315 data

wf3 → Need to CN process : Novellus & no densification may still need to work on the type of etching for oxide.

D1549 splits are actually as D1261, except D1261 was misprocessed. So D1549 is to repeat D1261.

Need to update PSC7223 based on D1168, D1315, D1549

④ Manufacturing / structural (see Z37223 PSC)

Need to collect L39 data : CD, overlay, cap-ox thickness, poly thicknesses

After D1114 lot → can get CD & overlay data

" " " → poly I/II, oxide thickness

" D0968 lot → Novellus

Etch issue is waiting for my 1st STR

⑤ Electrical

capacitor/resistor { D1549, D1315
Novellus, no undercut & pearl
capacitor matching whether it's structural or measurement issue
transistor —— same for nominal Leff
need to do # summary w/ Z70 lots

CMAT for undercut / no-undercut
final PEVAL verification (9 sites for production)

⑥ yield
—— sort program & results (D1549 rom code ?

was D1549, has the same rom code ? check it

(7) Reliability Test (mentioned on #1 above partially ?)

(8) Performance
→ Spice – at least the analog needs to get done
D1549 if the thickness is closed

Ring oscillator ? (can do it in design review)
(Esposito) speed is not affected by additional SLMs

Full spice for capacitor & resistors are not necessary

Who's doing what based on the Z37223 list for Limited release above :

Z37223 :

(2) D1168 lot report & roll-off
SGIR STR #2 priority (moved to Limited PR list)
(6) Reduce Vpp to 50mV or cap
(5) CMAT issue (CMAT CVCO are as important for converter devices)
D1114 ring oscillator summary (Lee - done)
WTC 37223
(1) add → D1114 PEVAL
(9) → New SLM verification
Final PEVAL verification (9 sites for production PEVAL)
(1) add → D1261 Review
(Add SLM 272 to PEVAL test (waffle type capacitors w/ guard ring)) part of this

(10) investigate scattering PMOS roll-off
SLM 200 current mirror fix (Scott)

(8) Design rule Margins

FPR = Full production Release (3/31/99) :

Deliverables

(4) capacitor test : QBD, 5V or ?V over some time & temp (stress test) for good capacitor (high BV ≃ 15V)
characterization

matching

③ Bipolar, transis[redacted] & poly 2
up to this pt, we don't have bipolar result yet.

LPR 2/15/99 ⟶ if final test program (is gated by qual

Z37235 : Z37125, Z37130

Z37235 contains all these 3 technology

FPR on Z37235 depends on L02 (Z37223 FPR date)

④ Product 1st Si (90305B, 90233C)

① - Need STR signed by Esposito → dated 2/17/99
if start on 1/4/99 don't have problem meeting the date 2/17/99.

- 90233 PEVAL @ M1, M2, ~~PEVAL~~ final M3 (transistor matching)

⑤ Qual lots related

② supreme simulation (BV + D1315)
⑧ HCI D1315 & modify to industrial record (Tower)
③ D1315 lot report
⑦ Leff resolution (PEVAL / New SLM)
④ 7125 margin analysis (rev. 1)

① PEVAL setup for 90305B / 90233C
caps
triple layer metals (one PEVAL @ each metal layer) for 90233C.
TLM
VT-match

⑤ Isubs reduction → maybe simulation
⑥ Snap back @ 5.5V → ~~6~~ → 6 → 7V (Marie McKencick? ~~Test~~ Product Eng @ campbell)
According to Tim, they pushed it back to 7V

⑩ SRP / simulation correct on final process
⑪ PMOS IOFF
⑫ PPLKG (random is working on this)

Delta W targeting
⑨ PSC structural, yield (metal 3 & planarization steps)

Deuterium (black burner)

Z37120
⑤ DW targeting (see PSC)
⑦ M1/M2 correlation
⑫ edit, DO 931 SRP
edit, HCi characterization
③ { final PSC (10 lot PEVAL)
PEVAL Summary (10 lot)
① Deliverables SP
④ L10 roll-off rpt for D1315
L10 fix mod III (NP_W)
⑧ I-V-T SLM 07/09/59 on final SLMs
Diode Leakage mod III
⑥ Well-anneal lot report

Z37229: FLASH -5V (polycide is part of flash)
-need NTP
we've done chisel cell characterization. We have several work for FLASH. It may not be flash, it may be mid-rom L45 (= enhancement rom, for 3V is not a problem, but for 5V it may be a problem because punch-thru is right at the edge).

Z37126: 3V mid rom (L45 enhancement)
-NTP

Z37128: 5V mid rom
-NTP

Z37122: 1.5V core → NTP,
go to there because of likelyhood for it to work
(polycide?)
High density SRAM (TV-cache memory for picture in picture)
1-4 Meg, require low power consumption
cell size 3 μm^2 right now
Most company used SRAM as their qual. because of complexity
Salicide -DNTP & a working ring oscillator compactness & # of fail bits

Z37229, Flash 5V [redacted], PSC rev 0.0, DR [redacted] 0.0, margins
- NTP → flow, financial
- test chip (Pete Manos)
- Need the most development (#1)

Z37126 } : tape out 02-99 #5
Z37128 }
- NTP
- BVDSS simulation for enhancement device; see if 3V, 5V are sufficient

~~Z37122~~ High Density SRAM (polycide?), Q3/99
- NTP
- Test chip
industry review (see what's out there?)
- #2

Z37122 : 1.5 core, completion / tape out year 2000
#4

Salicide : #3 development

- Set up a meeting for reviewing the Z37223 experiment L39/L40 on 1/4/99 afternoon. Key players: Esposito, Smythe & Cams. Do the L-10 D1315 report 2nd priority 1/13/99

- Shoot for Limited production release on 1/15/99 based on the data up to D1549 data.

- Capacitor characterization 1/13 - 1/25/99 (3rd priority)

- Capacitor matching - Mike does this the HP4146 doesn't have the resolution to measure capacitor matching. So Mike will need Lee's help to use PEVAL system.

* Update the split list

- L40 Etch:

A : Pearl (325 A) + Oxide + Poly 1

wfr 1 & 2

PEARL 325
oxide 375
Poly 1

B : Pearl (325A) + Oxide (~500A) + Poly 1

wfr 3

Pearl 325A
oxide ~500 A
Poly 1

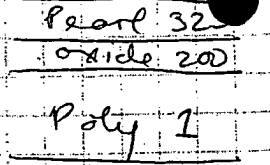
C : Pearl (325 A) + Poly 1

4, 5, 6, 7, 8
10, 11, 12, 13, 14
16, 17, 18, 19, 20, 21

Pearl 325
Poly 1

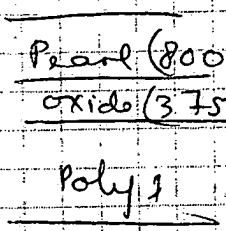
D : Pearl (325A) + oxide (~200A) + Poly 1

9, 15



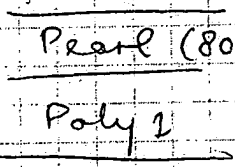
E : Pearl (800A) + Oxide (375A) + Poly 1

wfr 22



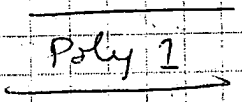
F : Pearl (800A) + Poly 1

wfr 23



G = Poly 1

wfr: 24, 25



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no undercut w/ pearl → will show leakage 13 & 14

9-12 with undercut, spacer might help & leakage

wfr 24 works, by default wfr 25 will work

22 - line width variability
800 A pearl

* Printers problem. Can not print out to all printers.

* Edited the D1114 Peral summary / Lot report, gave it back to Tim ~ 6:15 pm electronically

* Left ~ 6:30 pm

12/31/98, Th

* Arrive work ~ 8:05 am

* No meeting today because fab is down & Dob Adcock is not here. All of the unit process engineers & mod 3 engineers are off from christmas till Jan 4.

* Start working on the run-card for L39-oxide_L40 split list.

Mostly in the morning, downloading the runcards (Z37120 & 7223) from public folders. Inserting Z37223 process flow to Z37120.

Learnt from Mike how to eliminate the huge page number from the runcard. It is under: View → Normal.

* Tim came by & told me that I sent him the wrong version of D1114_summary file (from last night), so I resent him the correct version.
About 1 hr later, he signed off the D1114_summary report. I copied the report, gave the original to John-Smythe (Ask security to open his office — to drop off the report).

* Went asking Mike about any suggestion/preference to change # of wafers for a particular split of L39-oxide-L40 proposed splits. He said no preference. Then, Mike said, he thinks the proposed split will completely answer our questions: that is from D1315, we know wafers 15, 20 & 25 that DID NOT receive PEARL, but w/ undercut below poly 2, perform well, leakage is ~3 orders of magnitude lower than the rest of wafers 1-14, 16-19 & 21-24 that received pearl.

So, Even w/ undercut of oxide below poly 2 & NO Pearl, the capacitor's leakage performed well.
Undercut & pearl result in poor capacitor leakage.
This means pearl acts as an & the leakage path.

Initially D1315 split list and run-card were designed to have (resist strip only) NO OXIDE Removal @ L-39. But the run-card from the fab shows that all D1315 wafers received BOE oxide removal @ L39 (IPO Removal). This action was probably taken after they found out a large swing (0.01-0.02 um) in Leff caused by having oxide below pearl from D1261 & D1549 lots.

4

87L02 CAPACITOR OXIDE SPLIT

Wafer #	Capacitor Oxide (wait for data from D1549)	L39 IPD Removal	Cap. Spacer Oxide	Pre-clean	Capacitor Spacer Oxide Thick (A)	Spacer Etch	Pearl Deposition	L40 Etch	L40 DICD Splits	Hook Wafer
1, 2	Novellus	---	---	---	---	---	Y (325A)	A	Y	D1261: 18-20 D1549: 8 & 18
3	Novellus	---	RTP	---	---	---	Y (325A)	B	Y	
4	Novellus	---	RTP	---	---	A	Y (325A)	C	Y	
5, 6	Novellus	---	DEP	Y	1000	B	Y (325A)	C	Y	
7	Novellus	---	DEP	Y	2250	C	Y (325A)	C	Y	
8	Novellus	BOE	---	---	---	---	Y (325A)	C	Y	D1114-4
9	Novellus	BOE	RTP	---	---	---	Y (325A)	D	Y	
10	Novellus	BOE	RTP	---	---	A	Y (325A)	C	Y	
11	Novellus	BOE	DEP	Y	1000	B	Y (325A)	C	Y	
12	Novellus	BOE	DEP	Y	2250	C	Y (325A)	C	Y	
13, 14	Novellus	Dry Etch	---	---	---	---	Y (325A)	C	Y	
15	Novellus	Dry Etch	RTP	---	---	---	Y (325A)	D	Y	
16, 17	Novellus	Dry Etch	RTP	---	---	A	Y (325A)	C	Y	
18, 19	Novellus	Dry Etch	DEP	Y	1000	B	Y (325A)	C	Y	
20, 21	Novellus	Dry Etch	DEP	Y	2250	C	Y (325A)	C	Y	
22	Novellus	---	---	---	---	---	Y (800A)	E	Y	
23	Novellus	Dry Etch	---	---	---	---	Y (800A)	F	Y	
24	Novellus	BOE	---	---	---	---	N	G	Y	D1315-15
25	Novellus	Dry Etch	---	---	---	---	N	G	Y	

Spacer etch is a blanket etch → open etch

Main objective of the proposed splits
Minimal process modification from Z-70 process flow.

Questions to be answered:
Poor leakage capacitor performance on SLM 270 and emission around the edges of capacitor from hypervision experiment suggest that we have the following possibility of leakage path:

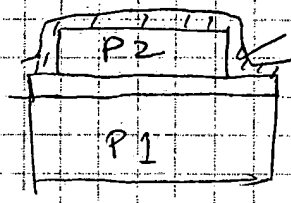
1. Undercut of capacitor oxide using BOE. This issue is investigated by implementing spacer oxide (RTP vs. DEP—1000 vs. 2250 A), dry/wet etch oxide and/or not removing oxide at L39.
2. Contamination of Pearl and capacitor oxide in undercut region. This issue is investigated by implementing spacer oxide step and not removing oxide at L39.
3. Pearl layer touching both poly 1 and poly 2. This issue will be resolved by not removing the oxide at L39.

The swing effect remains on the wafers that receive no oxide removal step. This effect is also investigated in the proposed splits:

1. By increasing pearl layer thickness to 800A. This step requires some photo and CMP development.
2. By eliminating pearl layer. This step will reduce the line width control of L40.

Note for L40 Etch:
A = Pearl (325A) + Oxide (375A) + Poly 1
B = Pearl (325A) + Oxide (~500A) + Poly 1
C = Pearl (325A) + Poly 1
D = Pearl (325A) + Oxide (~200A) + Poly 1
E = Pearl (800A) + Oxide (375A) + Poly 1
F = Pearl (800A) + Poly 1
G = Poly 1

Mike is thinking about patterning some steps that have oxide ~~pearl~~ to prevent pearl from touching both Poly 1 & 2, yet ~~not~~ reducing / eliminating the swing effect @ L40 (caused by pearl on oxide) → poor line-width control @ L40.



⇒ swing effect

D1261 & D1549

{ cost effective
easy to implement
improvement of certain factor

These 3 factors were in our conversation around room: like what kind of steps one has to take to pattern an idea. It is not necessary to convert the idea to a practice. In other words, it is not necessary to have experimental data to support your idea.

According to Mike, if he has an idea, he would file an ~~id~~ invention disclosure form & put his name on it. From places that he has worked, some people would go around asking questions about what he/she thinks about how to resolve a problem & then file a pattern that wasn't even his/her own idea. So, want to be careful & discrete when asking question that might be helpful to your idea w/o disclosing your idea.

Typical turn around time to have a bonus from an idea that accepted into a pattern is about 1 – 2 years. During this time if you get laid off, quit or fired, you won't receive the bonus ($$) likely.

Generally, after you file an invention disclosure form & submit a few pages that describe when & how you come out w/ the idea + other details, it gets sent to corporate office & review by a lawyer to see if it is worth patterning or to check if the idea has been used. Then the lawyer will rewrite your original idea to cover as many wide possibility as possible w/ legal binding to it & resend it back to you to review. At this pt, you won't even recognized the original report you wrote, but the basic idea is there. Then, once you approve it, send it back to the lawyer, & the lawyer will send it to ? pattern office. If accepted, you will get from ~ $500 → $1,000 / pattern.

From our lengthy conversation about patterning an idea, suddenly the idea to reduce the oxide under-neath pearl layer struck my mind.
Suddenly, I started thinking about the basic optical properties of pearl film on oxide.

I told Mike that I do not know what λ (wavelength) they use @ L-40 exposure. I know it is UV light, but don't know exactly @ what λ. Also, at what λ, pearl layer starts absorbing the light. similarly for the oxide
Interaction of light to pearl & oxide film.
How light changes phase @ every-interface & interferences affect, etc.
optically
They are many things that I don't know @ this pt.

But it sure sounds like reducing the oxide thickness down to 20 – 50°A might reduce the swing effect, yet provide the insulation of pearl from poly 1 & 2.

So, Mike suggested that I discretely ask this question to Brett Lowe.
The preferred technique to etch the oxide is dry etch, although BOE might work too.
We leave it at this pt, right now. I definitely will find out more about the rate of success for this idea later.

We also talked about the possibility of using oxynitride as the alternative mtl. The difference between pearl & oxynitride is different growth condition in the same chamber. pearl is Si-rich w/ some O_2 & N_2.
Oxynitride is NOT Si-rich.
If oxynitride has been used by some-else for line-width control, then oxynitride may be another option.
If it has NOT been used, need a lot of development.

* the rest of afternoon, worked on the run-card based on the split list in previous page.

Obtained the exposure & DICD values from Mike @ ~5:35 pm
The values used are the same as the ones used in D1315 for L4C-DICD split.
Got the general/most run-card done.
* Send out emails to plan a meeting to review an SDE on 1/4/99 at 2:30
* Left ~6:10 pm

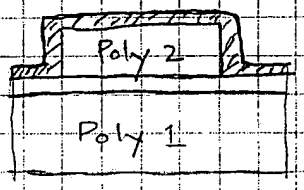
1/3/99, Su

- Came to work around 4 pm
- Answered personal emails
- Printed out 1999 calendar
- Work on minor details (line, ball alignment. size of font, etc) ⇒ then printed out the run-card
- Wrote down what I did on 12/31/98.

1/4/99, 'M:

* Arrive work ~ 8:10 am
* Attend Monday meeting
* Send out email to inform the location for meeting at 2:30 pm today. It is going to be in blue room. I invited: Tim Carns, M. Westphal, Lee Debtaker, John Esposito, John Smythe, Bee Kickel, Min Huang, Jon Daley, John Horrath, Mitch Mooney, Brett Lowe, Jim Shaw, John Gdd & Steve Buffat.
* Will work on SDE presentation (see split list on 12/31/98)

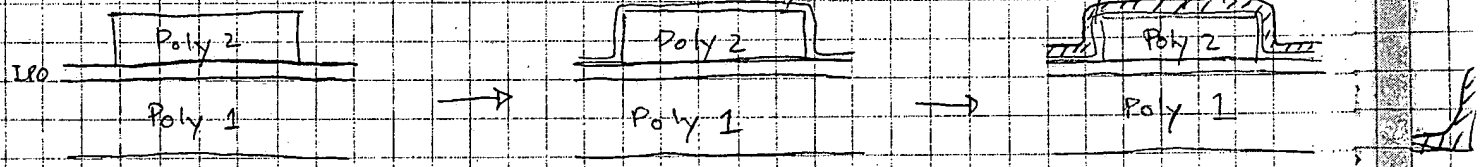
Wafer 1 & 2



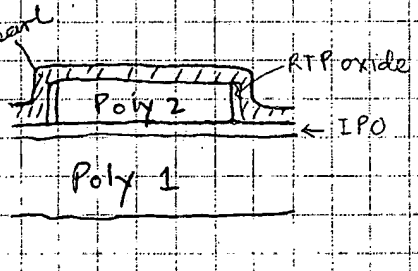
Poly 2 is defined at L39
oxide & poly 1 are defined at L40

L40 etch removes pearl (325A) + oxide + poly 1

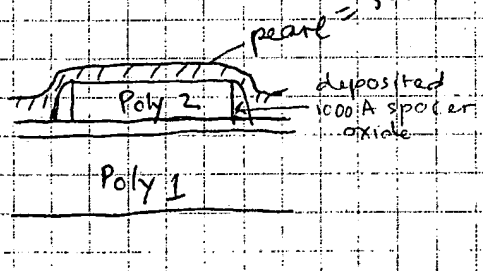
wafer 3



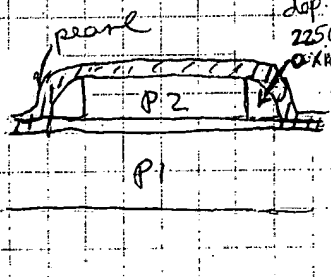
wafer 4



wafer 5



wafer 6



wafers 1 → 6 : Pearl do not contact both P1 & P2 at the same time

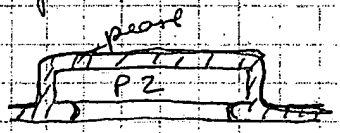
We know this structure will dramatically improve capacitor performance (D1261 & D1549). But swing effect at L40 arises by having pearl on oxide.

L8

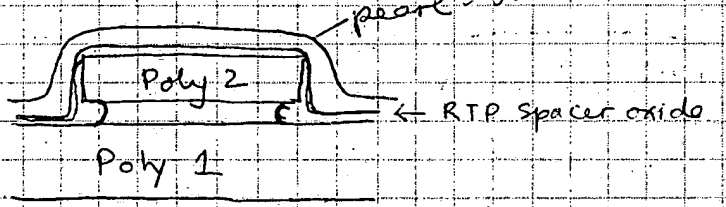
Wafers 1-6 will also tell us whether swing effect @ L40 will get worse or better by having thicker oxide underneath pearl.

Wafers 8 → 12 : Novellus oxide & BOE at L39
Pearl contacts both poly 1 & 2.

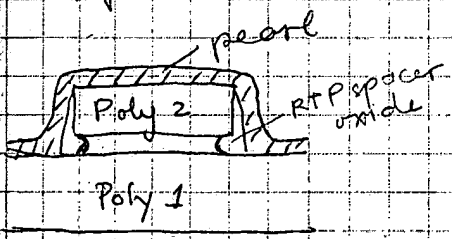
wafer 8:



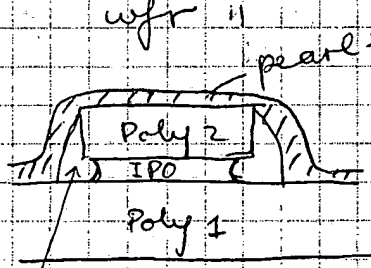
wafer 9:



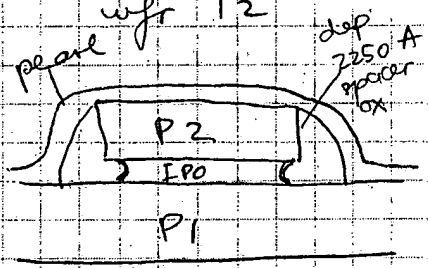
wafer 10



wfr 11

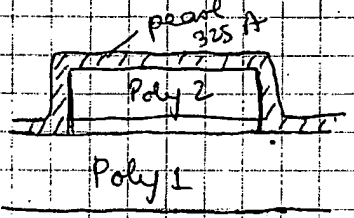


wfr 12



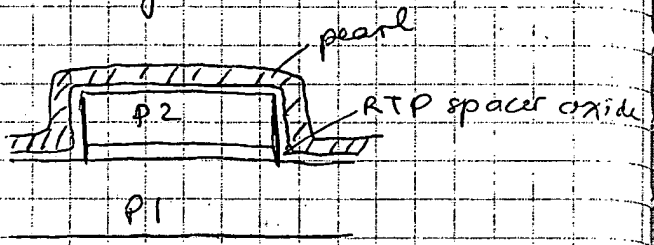
wafers 13 → 21 : Novellus capacitor oxide, dry etch IPO removal

Wfrs 13 & 14



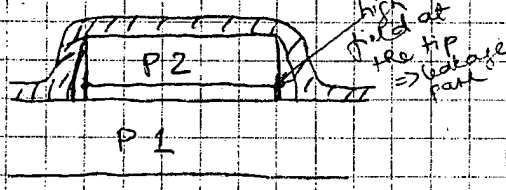
Pearl touches both P1 & P2

wafer 15

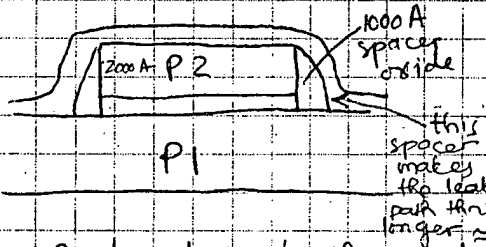


RTP spacer oxide provides as an insulation for pearl to contact both P1 & P2

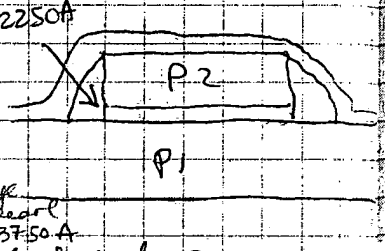
Wfrs 16 & 17
RTP spacer ox & then etched



Wfrs 18 & 19
1000A dep. sp. oxide



Wfrs 20 & 21
2250A dep. sp. oxide

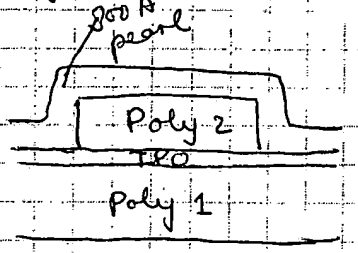


For the wafers where pearl touches both poly 1 & poly 2, the spacer might help reducing the leakage path, but capacitor performance is not optimized because pearl is the leakage path.

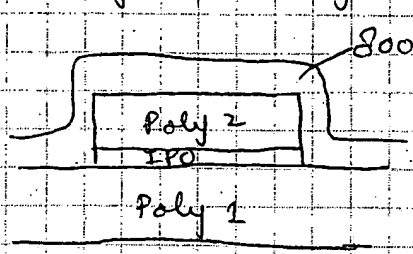
Initially without spacer (wfrs 13 & 14), : IPO thickness ~ 375 A.
Later, with spacer (wfrs 16 → 21), the total leakage path is longer (from 375 A = IPO to ~ 3750 A). So the leakage path thru pearl is longer, which may improve or reduce cap-leakage by ~ 1 order of magnitude assuming linear relation-ship of the oxide thickness to the leakage. But, again the capacitor performance is not up to its max as long as pearl touches both poly 1 & poly 2.

* wfrs 22 & 23 : Novellus oxide & 800 A pearl

wfr 22 : NO IPO Removal @ L39

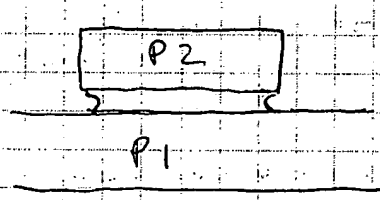


wfr 23 : dry etch oxide

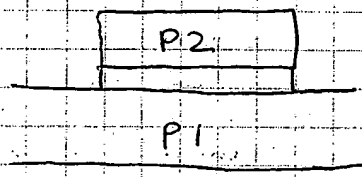


wfrs 24 & 25 : Novellus cap. oxide, BOE vs. Dry Etch, NO PEARL

wfr 24, BOE



wfr 25, dry etch



** Meeting @ 2:30 - 3:30 pm to review an SDE for capacitor (L39-oxide-L40)

Here is the proposed splits, more or less reflect our discussion from last year (a few wks ago). The objective of the splits is to answer the leakage path, whether it is caused by undercut oxide using wet etch (BOE), contamination of pearl and oxide in undercut region; or pearl touching both poly 1 & 2. @L40 due to pearl on oxide.
The swing effect is also investigated in this split.

This split was initially proposed before having D1315 data which show pearl layer contacting both poly 1 & 2 acts as the leakage path even w/ undercut oxide.

Correction at L-40 etch was made for wafers 4 - 7. This correction was pointed out by Jim Shaw

With that, the floor is open for discussion, comment, suggestion or objection that all of you have

Attendees: Deb Acock, Jean Adams, Steve Buffat, John Horvath, Bea Kickel, J. Smythe, T. Carns, M. Westphal, Mitch Mooney, Shelly Dove & L. Debruler

The meeting went pretty well, although it seems that there is a need to go over the split objective by ~~split~~ column to the audience, even though the split list was already sent out to them w/ the meeting notice.

There is almost no objection. D1315 ~~data~~ was also presented i.t. of Leakage 270 vs. wafer # where the boxplot shows all wafers (15, 20 & 25 having no pearl & no OPC) have several order of magnitude (3-5 orders) lower in leakage value than wafers that received pearl & OPC. Tim wants Mike to present that data on Wednesday (1/7/99).

There are some minor changes on the split list, see next page.

After meeting, Tim wants to go over the run-card w/ J. Horvath, M. Westphal, J. Smythe, B. Kickel & Deb Acock. I told him that I can get the run-card done in ~ 1 hr w/ the right wafer #.

- Send out another meeting notice to invite those people to review the run-card @ 4:15 pm in Blue room to review run card for the split list presented a few hrs earlier. All came, except Bee who later drop by briefly to talk to Deb Acock.

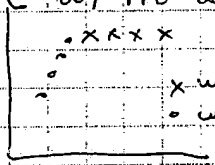
- At this meeting, additional experiment is added: The effect of dry resist strip vs. no dry strip at L39 for IPO removed w/ BOE & dry etch techniques (wfrs 1 & 12; 20 & 21 → see the attached split list on next page).

- Tim also wants me to plot Leff by exposure for different splits; for D1315 lot: pearl vs. no pearl; for D1549 by different L-40 etch. This plot will determine the exposure & DICD for L40 in the new ℘ STR. (my 1st STR).

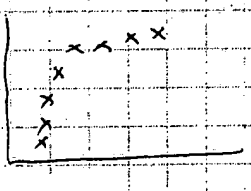
Want all wafers to have Leff in non-roll off & roll-off region.

In D1315, we have most wafers (11-25) data in non roll-off region; only the ones that receive no pearl shows roll-off region w/ no data in non-roll off region.

data



So, we want this, one wafer has data in roll-off & non-roll off region:



- No PEVAL @ M1

- Attach PEVAL sheet to the run-card, ask Lee about this

- J. Smythe, the RTP spacer oxide thickness is ~ 50A. I am glad to hear this because this 50A may be enough to provide an insulation for pearl from contacting both polys. Although my initial idea was not growing any spacer oxide, it was to use the IPO & etch it slightly incomplete to leave ~ 20-50A of oxide on poly 1. But this might work too.
w/ spacer oxide

* From ~5:15 → 7:30 pm
Make changes on the run-card & split list.

I also talked to Mike about my temptation to try AR inner oxide (instead of completely removing it or leave it there), so I change the wafer # to have 2 wafers on Novellus, Dry strip & Dry etch, RTP (spacer oxide), no spacer oxide etch, pearl (325A).

* From run-card review (2nd time: Tim, John, Bob & I, Bee couldn't make it because of 1:15 pm design review meeting),
- I learnt from Smythe that white space in L02 w/ the waffle's space is as big as L88 chip.

- punch-through step @ L40 Etch is designed to remove 100A + 325? 375A oxide.

87L02 CAPACITOR OXIDE SPLIT

87L02 CAPACITOR OXIDE SPLIT

Wafer #	Capacitor Oxide	L39 IPD Removal	Cap. Spacer Oxide	Pre-clean	Capacitor Spacer Oxide Thick (A)	Spacer Etch	Pearl Deposition	L40 DICD Splits	L40 Poly Etch	Hook Wafer
1	Novellus	---	---	---	---	---	Y (325A)	Y	A	D1261: 18-20 D1549: 8 & 18
2	Novellus	---	RTP	---	---	---	Y (325A)	Y	B	
3	Novellus	---	RTP	---	---	A	Y (325A)	Y	A	
4	Novellus	---	DEP	Y	1000	B	Y (325A)	Y	A	
5	Novellus	---	DEP	Y	2250	C	Y (325A)	Y	A	
6	Novellus	Dry Strip, BOE	---	---	---	---	Y (325A)	Y	C	D1114-4
7	Novellus	Dry Strip, BOE	RTP	---	---	---	Y (325A)	Y	D	
8	Novellus	Dry Strip, BOE	RTP	---	---	A	Y (325A)	Y	C	
9	Novellus	Dry Strip, BOE	DEP	Y	1000	B	Y (325A)	Y	C	
10	Novellus	Dry Strip, BOE	DEP	Y	2250	C	Y (325A)	Y	C	
11, 12	Novellus	NO Dry Strip, BOE	---	---	---	---	Y (325A)	Y	C	
13. 14	Novellus	Dry Strip, Dry Etch	---	---	---	---	Y (325A)	Y	C	
15, 16	Novellus	Dry Strip, Dry Etch	RTP	---	---	---	Y (325A)	Y	D	
17	Novellus	Dry Strip, Dry Etch	RTP	---	---	A	Y (325A)	Y	C	
18	Novellus	Dry Strip, Dry Etch	DEP	Y	1000	B	Y (325A)	Y	C	
19	Novellus	Dry Strip, Dry Etch	DEP	Y	2250	C	Y (325A)	Y	C	
20, 21	Novellus	NO Dry Strip, Dry Etch	---	---	---	---	Y (325A)	Y	C	
22, 23	Novellus	---	---	---	---	---	Y (800A)	Y	E	
24	Novellus	Dry Strip, BOE	---	---	---	---	N	Y	F	D1315-15
25	Novellus	Dry Strip, Dry Etch	---	---	---	---	N	Y	F	

87L02 CAPACITOR OXIDE SPLIT

Main objective of the proposed splits
Minimal process modification from Z-70 process flow.

Questions to be answered:
Poor leakage capacitor performance on SLM 270 and emission around the edges of capacitor from hypervision experiment suggest that we have the following possibility of leakage path:

1. Undercut of capacitor oxide using BOE. This issue is investigated by implementing spacer oxide (RTP vs. DEP—1000 vs. 2250 A), dry/wet etch oxide and/or not removing oxide at L39.
2. Contamination of Pearl and capacitor oxide in undercut region. This issue is investigated by implementing spacer oxide step and not removing oxide at L39.
3. Pearl layer touching both poly 1 and poly 2. This issue will be resolved by not removing the oxide at L39.

The swing effect remains on the wafers that receive no oxide removal step. This effect is also investigated in the proposed splits:

1. By increasing pearl layer thickness to 800A. This step requires some photo and CMP development.
2. By eliminating pearl layer. This step will reduce the line width control of L40.

The effect of dry resist strip vs. no dry strip at L39 is also investigated for IPO removed with BOE and Dry Etch techniques.

Spacer Etch:
A = ~50A RTP Spacer Oxide
B = 1000A Deposited Spacer Oxide
C = 2250A Deposited Spacer Oxide

L40 Etch:
A = Pearl (325A) + Oxide (375A) + Poly 1
B = Pearl (325A) + Oxide (~425A) + Poly 1
C = Pearl (325A) + Poly 1
D = Pearl (325A) + Oxide (~50A) + Poly 1
E = Pearl (800A) + Oxide (375A) + Poly 1
F = Poly 1

1/5/99, Tuesday

- Arrive work ~8:15am
- Read emails, no mail
- Write down the stuff I did from yesterday afternoon
- Work on the split list, mainly to arrange wafers # accordingly
- Update / change the run-card
- Attend PI 9:30 meeting in West conference room → 11am
- Ask Tim about the wafers (Loc. 630 L39 cap etch) that do not receive dry resist strip, the resist removal step in included in the IPO removal BOE step.
- update the run-card & STR (ask wendy how to edit run-card : use Query, type in Serial #, hit escape, hit update, this will bring you to edit move — once added information is typed in, hit escape, then Table to bring to 2nd table, Query, Serial #, escape, update, etc.)

  Got all of this done ~3pm

  Will work on plotting Leff vs. exposure

→ In this PI meeting, Tim mentioned that we are going to use SRAM chips as our test chip for all future development & products. Because SRAM is the most restricted device in terms of size, etc & thus performance to determine how well our design, device & processes are. Basically, using SRAM will tell us the worst case scenario memory

Tim also presented several future road-map. I wrote down a few:

FLASH : John

Mask ROM converts to FLASH

How many ROM parts would be converted, if any?

Z37123/8/ (3V/5V Late ROM - L45) : Tim

L45 : contact mask

L50 : define contacts for the ones used & the ones not used get knock off.

Salicide John

1. do we have any products requiring high speed?
2. what is the current maximum speed capability for Z37130 & Z37125 (50 MPs, 70 MPs, ??? or more)

MPs = million per second

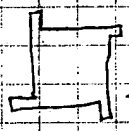
3. Will this be necessary for high density SRAMs?

Non-volatile testchip
CMOS —
Analog —

ETB?

Difference between P2_W_05 vs. Leff per Mike W.:

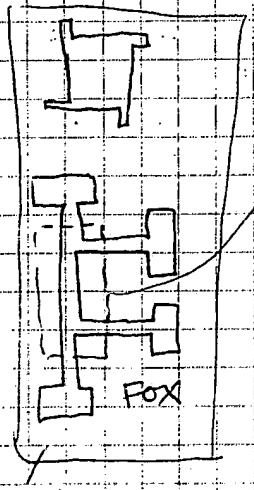
P_2_W_05 = physical gate width, electrically determined poly line-width



van-der-paw to determine sheet ρ to calculate P_2-W_05

Leff = channel length under the gate.

P_2_W_05 & Leff are measured from separate SEM.

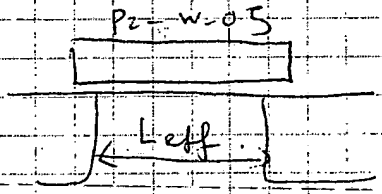


1 SEM

P_2_W_05 is measured on field-oxide. other company/other device may measure P_2_W_05 on active area

poly on active area to determine P_2_W_05 variation from the bottom of active area to the top.

Leff is measured from transistor (during SEM)



DICD - Leff ≈ 0.09 μm.

0.1 μm spec window off from roll-off Leff from D1114

Because of new-rom code which has NO waffle, poly etch would be etched differently

D1549 hp files :

		wafer #
strd1549	→	1
strd1549_a		2 & 3
strd1549_b		4 & 5
strd1549_c		6
strd1549_d		7
strd1549_e		7 (suppose to be 7), but in hpfile it is 8
_f		8 & 9
_g		10
_h		11
_i		12
_j		13
_k		14
_l		15
_m		16
_o		17
_p		18
_q		19
_r		20
_s		21
_t		23
_u		22
_v		24
_w		25
_x		

* generate a table w/ all of the hp files in col 1

* to generate a giant table that contains all of the hp files, do this command in RS1

#build ("tablename", col#, "new tablename")

example:

#build ("hpfiles", 1, "D1549all")

RS1, the perval file:

col0 = PERVAL_hpfiles	col1 = wafer #
strd1549_e	8
	8
	8
strd1549_f	8
	9

want to change 8 to 7 for strd1549_e do this command @ RS1

strd1549_e	7
	7
	7

Set col 1 where col 0 = "strd1549_e" to 8

or

Set col 1 where col 0 = "strd1549_e" and col 1 = "7" to "8"

or

L40 [redacted] splits

D1315

Exposure	DICD Target	Leff Target	Actual DICD (wfr13)
1500	0.472	0.382	0.486; 0.46; 0.468
1650	0.425	0.335	0.431; 0.418; 0.447
1975	0.377	0.287	0.371; 0.359
2290	0.32	0.23	0.307; 0.315

Set: 1500 → DICD ~~>~~ 0.45
1650 → 0.38 < DICD < 0.45
1975 → 0.34 < DICD < 0.38
2290 → DICD < 0.34

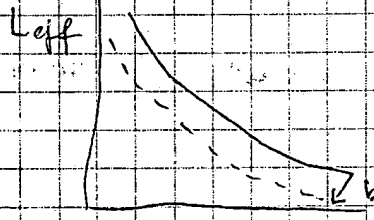
D1549

wfr 17 & 18

Exposure (J/m²)	DICD Target	Actual DICD 17	Actual DICD 18
1500	0.472	0.457;	0.45
		0.473;	0.462
		0.477;	0.494
1650	0.425	0.441;	0.459
		0.429;	a428
		0.393;	0.359
1975	0.377	0.371;	0.363
		0.376;	0.352
2290	0.32	0.32;	0.31
		0.32;	0.299

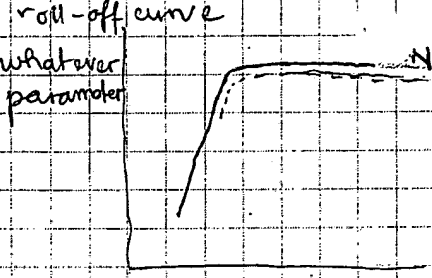
→ Set col 7 where col 3 ≥ 0.38 and col 3 < 0.45 to "1650"

Anticipated Leff behavior by changing L40 mask (waffle to non-waffles)



DICD - Leff = 0.09 ~~else~~

because of a new rom code which has non-waffle at L-40, the poly (at L40) will get etched differently → lower Leff.



DICD
0.472 →

≥ 0.47
0.40 — 0.45 1960
0.34 — 0.39 0.40 2190
< 0.35

* Leff ~ 8 pm

1/6/99, Wed

- Arrive Work ~8:10 am
- Read & send emails
- make D1315 plots } Leffnc vs L40 exposure , Leffnc vs pearl/opc
  poly-line width vs. L40 exp , polywidth vs. pearl/opc

D1C0 = Leff + 0.09

0.472 - 0.09 = Leff

Target

Exp=1500 Leff = 0.382

Exp = 1650 Leff = 0.335

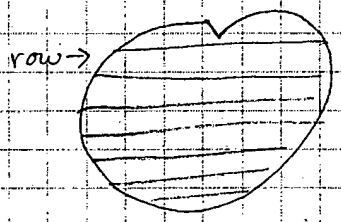
= 1975 Leff = 0.287

= 2490 Leff = 0.23

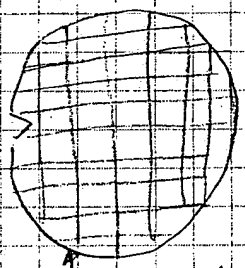
0.472	0.425
0.09	0.09
0.382	0.335
0.32	0.377
0.09	0.09
0.23	0.287

D1315

L40 exposure



PE-VAL



(1, 2)